

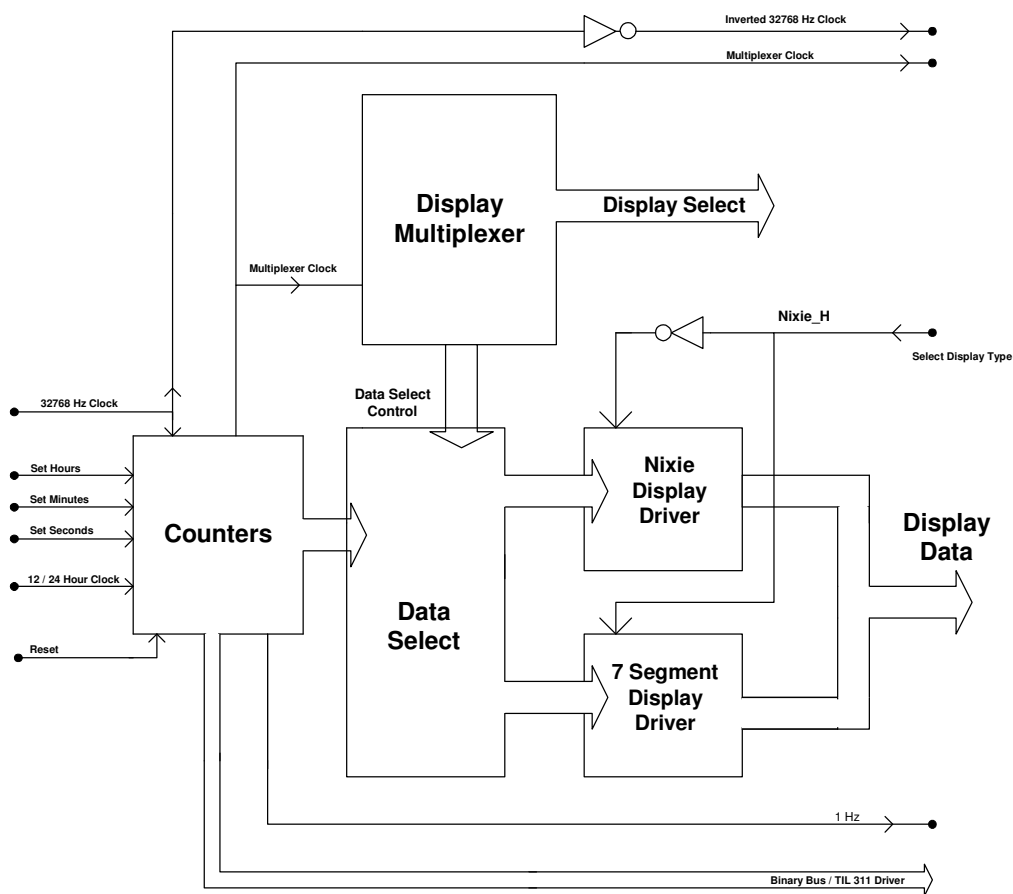
# DATA SHEET FOR CLOCK SUB SYSTEM DEVICE CLKSS-N7

## Introduction

The CLKSS is a complete timing system for a clock. The -N7 suffix means that the output is switchable between a form suitable for Nixie tubes and a form suitable for 7 segment displays.

All that is required to construct a clock is an accurate (crystal derived) 32768Hz timing signal, 3 push button switches (to set the time) and a suitable display arrangement (see application circuits).

## Block Diagram



## Basic Function

### Timing generation

The device divides down the 32768Hz clock internally. The correct time is set using 3 separate inputs, one for seconds, one for minutes and one for hours. When the time is being set, the normal counter input is disabled. Rudimentary digital switch de-bounce is performed within the device on the 3 setting inputs. Recommended practice though is to further reduce switch bounce by following the switch

configuration shown in the application circuit. When setting the time, the display will increment at a rate of 2 Hz.

## **Display Driving**

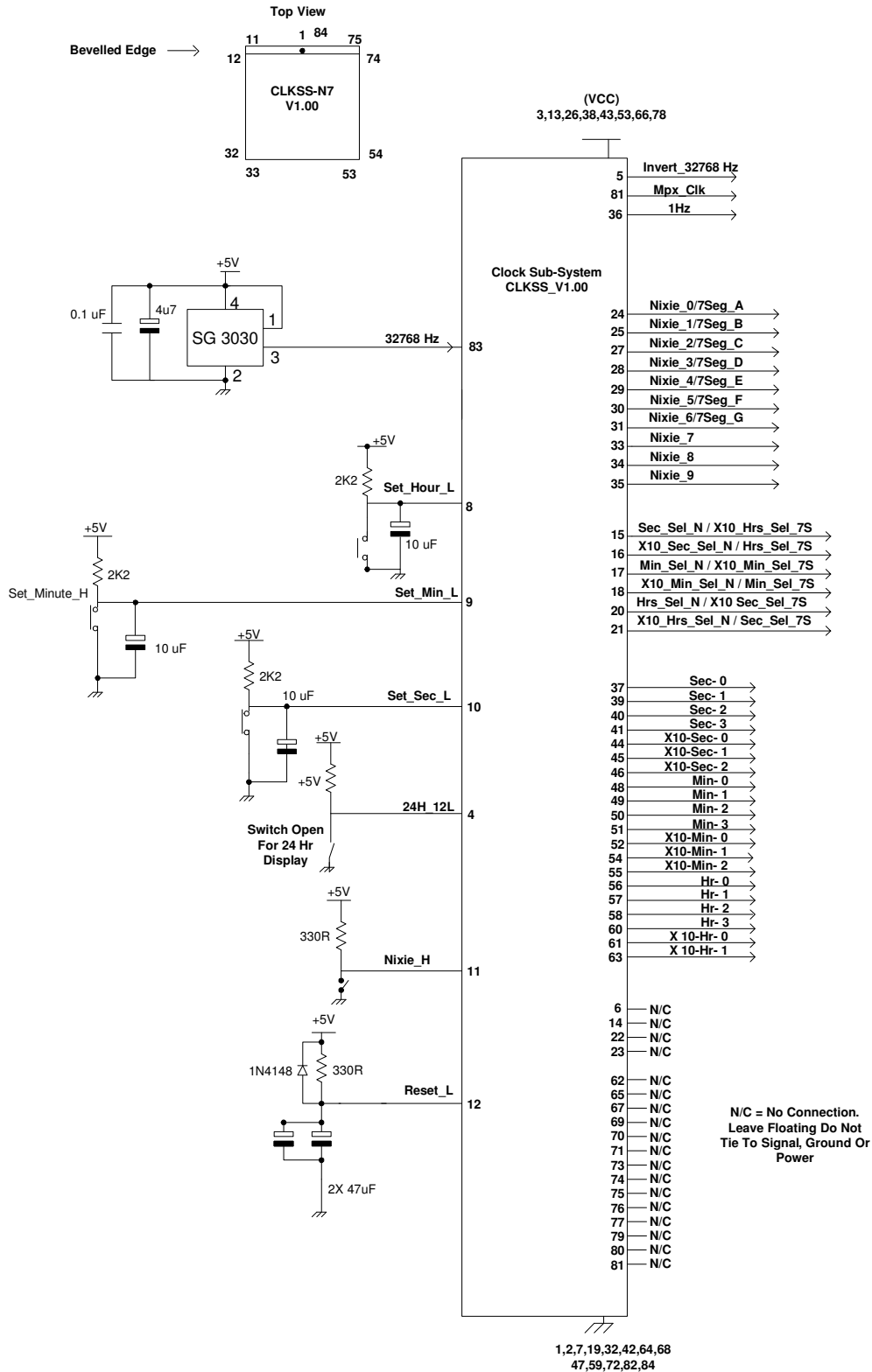
One of the central criteria for the Nixie output stage design was to avoid having to use hard-to-find Nixie tube driving IC's. The reference design shows how the Nixie tubes can be driven using cheap discrete transistors.

To minimise complexity of wiring, it was decided to implement multiplexing circuitry on both the Nixie and 7 segment driving circuits. In this way only one Nixie tube is lit at a time and all Nixie tubes are fed from the same "number bus". The switching rate (set by the multiplexer clock) is set at such a value so that the human eye sees all tubes alight simultaneously.

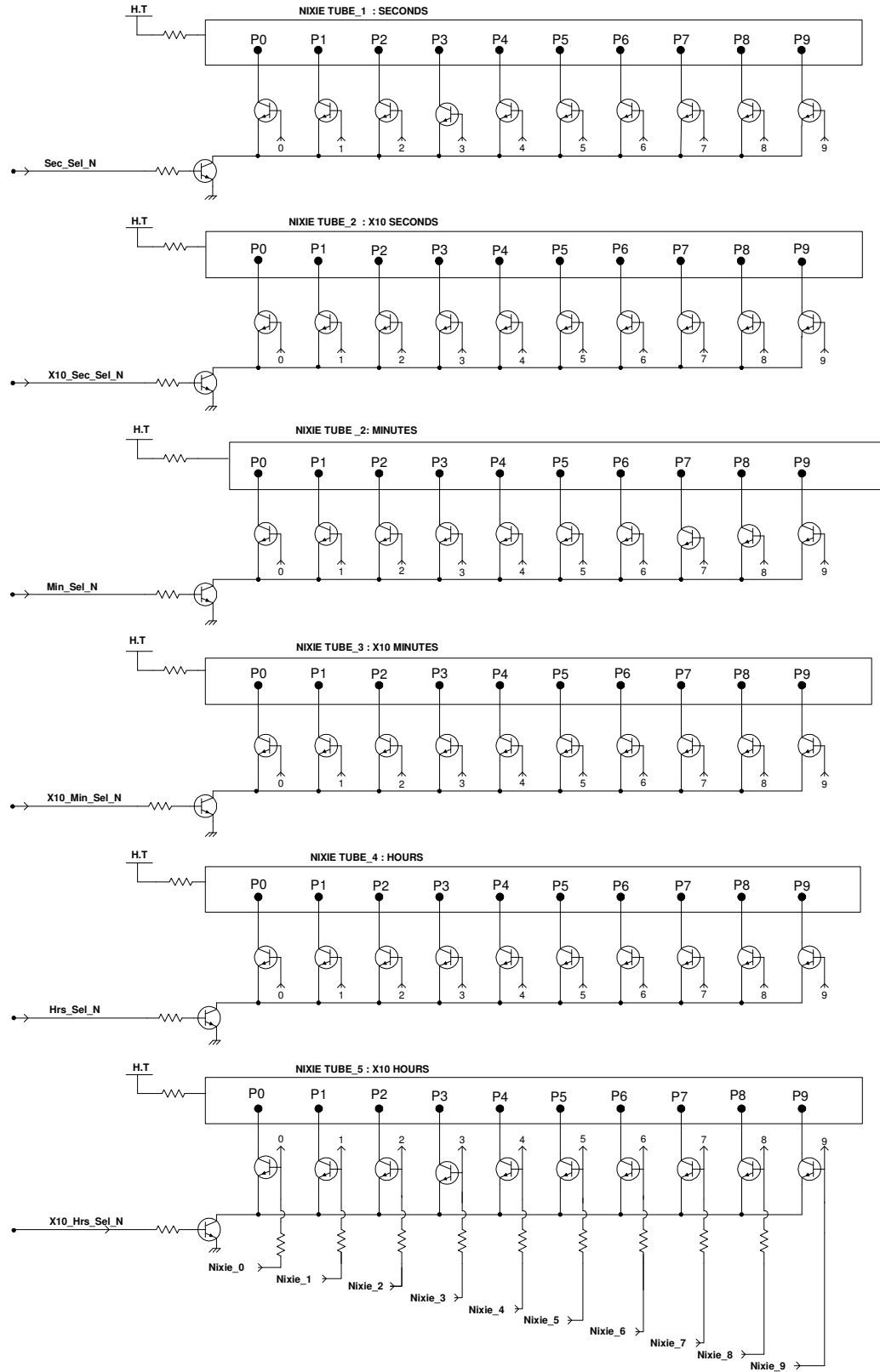
Using this arrangement, the entire 6 Nixie (fully expanded) display only requires 16 signals from the device ( 10 lines to represent the display digits 0 to 9 and a further 6 lines to switch on each Nixie in turn). If you only require a display of 4 Nixies (i.e you don't want to display seconds) simply omit the 2 "second" and "X10 second" Nixie tubes and associated circuitry. Tie the "Set\_Sec\_L line permanently high.

The 7 segment driver requires only 14 lines (7 to represent the 7 segments of the displays and 6 to switch each display on in turn)

# Application Circuits



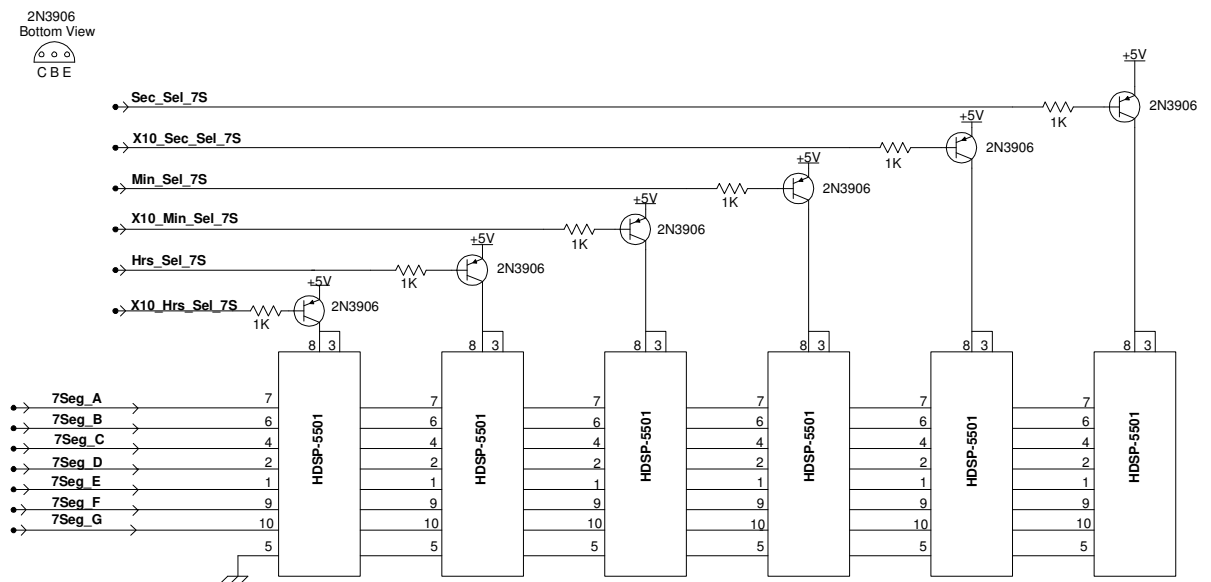
# Nixie Driving Arrangement



## Design Notes

1. The Value of HT and HT resistor are dependent on the Nixie tube used.
2. Transistors should be of a NPN switching type, able to withstand the value of HT used. For most purposes the MPS-A42, will be fine, they can withstand up to 300V between collector and emitter.
3. The base resistors of the transistors should be chosen so that the transistor goes into saturation and switches “cleanly”.
4. Set Pin 11 (Nixie\_H) to logic “1” (+5V).
5. Please note the display enable “bus swap” between the Nixie and 7 Segment display modes. The reason for this is pure laziness on my behalf, it meant I could test the CPLD using existing circuitry, without having to re-built test rigs – Apologies for any inconvenience caused !

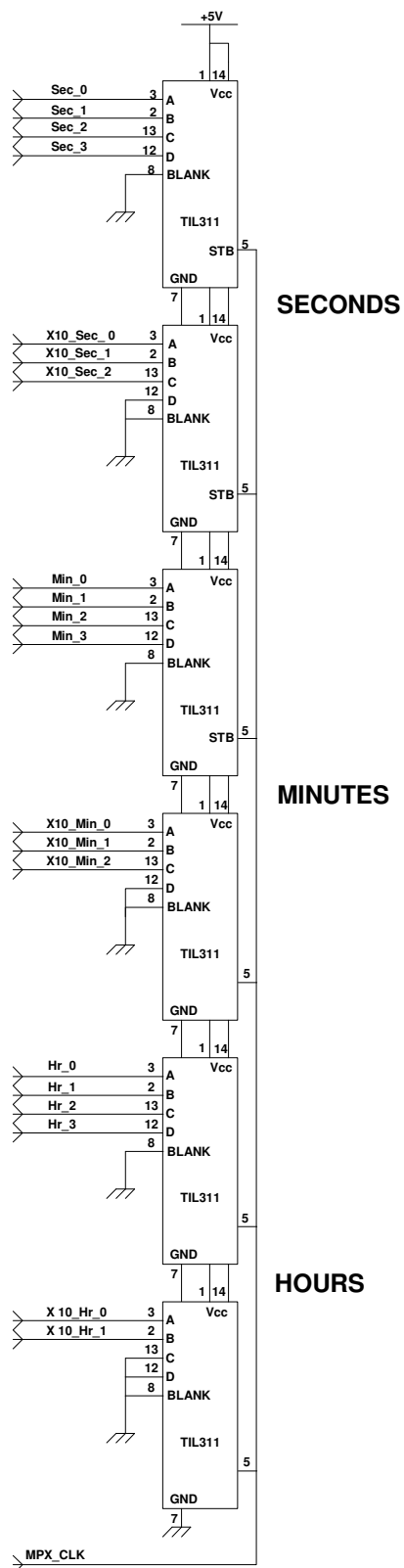
## 7 Segment Driving Arrangement



## Design Notes

1. Any switching or general purpose transistor should work – Ensure that the base resistor is chosen so as to drive the transistor into saturation.
2. Set Pin 11 (Nixie\_H) to logic “0” (0V).
3. Please note the display enable “bus swap” between the Nixie and 7 Segment display modes.

## Driving TIL 311 Displays From The Binary Output Bus



## Pin Descriptions

Pin	Type	Description
1	PWR	GND
2	PWR	GND
3	PWR	+5V
4	I/P	24H_12_L : Set to logic "1" for 24Hr Clock "0" for 12
5	O/P	INVERT_32768Hz : Inverted I/P Clock
6	N/C	
7	PWR	GND
8	I/P	Set_Hour_L : Logic "0" To Set Hours
9	I/P	Set_Minutes_L : Logic "0" To Set Minutes
10	I/P	Set_Seconds_L : Logic "0" To Set Minutes
11	I/P	Nixie_H Logic "1" O/P To Be Nixie Type "0"=7Seg
12	I/P	Reset_L : Logic "0" To Clear Counters, "1" for run.
13	PWR	+5V
14	N/C	
15	O/P	Sec_Sel_N / X10_Hrs_Sel_7S : Enables The "Second" Display For Nixie Usage Or Enables The "X10 Hrs" Display For 7 Segment Display use. (Dependant On State Of Pin 11)
16	O/P	X10_Sec_Sel_N / Hrs_Sel_7S (See Above Description)
17	O/P	Min_Sel_N / X10_Min_Sel_7S (See Above Description)
18	O/P	X10_Min_Sel_N / Min_Sel_7S (See Above Description)
19	PWR	GND
20	O/P	Hrs_Sel_N / X10_Sec_Sel_7S (See Above Description)
21	O/P	X10_Hrs_Sel_N / Sec_Sel_7S (See Above Description)
22	N/C	
23	N/C	
24	O/P	Nixie_0 / 7Seg_A : Nixie Digit 0 or 7seg A ( See Pin 11)
25	O/P	Nixie_1 / 7Seg_B : Nixie Digit 1 or 7seg B
26	PWR	+ 5V
27	O/P	Nixie_2 / 7Seg_C : Nixie Digit 2 or 7seg C
28	O/P	Nixie_3 / 7Seg_D : Nixie Digit 3 or 7seg D
29	O/P	Nixie_4 / 7Seg_E : Nixie Digit 4 or 7seg E
30	O/P	Nixie_5 / 7Seg_F : Nixie Digit 5 or 7seg F
31	O/P	Nixie_6 / 7Seg_G : Nixie Digit 6 or 7seg G
32	PWR	GND
33	O/P	Nixie_7 : Nixie Digit 7
34	O/P	Nixie_8 : Nixie Digit 8
35	O/P	Nixie_9 : Nixie Digit 9
36	O/P	1Hz Signal
37	O/P	Sec_0 : Binary Timing Bus (0) LSB
38	PWR	+5V
39	O/P	Sec_1 : Binary Timing Bus (1)
40	O/P	Sec_2 : Binary Timing Bus (2)

41	O/P	Sec_3 : Binary Timing Bus (3)
42	PWR	GND
43	PWR	+5V
44	O/P	X10_Sec_0 : Binary Timing Bus (4)
45	O/P	X10_Sec_1 : Binary Timing Bus (5)
46	O/P	X10_Sec_2 : Binary Timing Bus (6)
47	PWR	GND
48	O/P	Min_0 : Binary Timing Bus (7)
49	O/P	Min_1 : Binary Timing Bus (8)
50	O/P	Min_2 : Binary Timing Bus (9)
51	O/P	Min_3 : Binary Timing Bus (10)
52	O/P	X10_Min_0 : Binary Timing Bus (11)
53	PWR	+5V
54	O/P	X10_Min_1 : Binary Timing Bus (12)
55	O/P	X10_Min_2 : Binary Timing Bus (13)
56	O/P	Hr_0 : Binary Timing Bus (14)
57	O/P	Hr_1 : Binary Timing Bus (15)
58	O/P	Hr_2 : Binary Timing Bus (16)
59	PWR	GND
60	O/P	Hr_3 : Binary Timing Bus (17)
61	O/P	X10_Hr_0 : Binary Timing Bus (18)
62	N/C	
63	O/P	X10_Hr_1 : Binary Timing Bus (19)
64	N/C	
65	N/C	
66	PWR	+5V
67	N/C	
68	N/C	
69	N/C	
70	N/C	
71	N/C	
72	GND	
73	N/C	
74	N/C	
75	N/C	
76	N/C	
77	N/C	
78	PWR	+5V
79	N/C	
80	N/C	
81	O/P	Mpx_Clk : Multiplexer Clock (4096 Hz)
82	PWR	GND
83	I/P :	32768Hz : Input Timing Clock (Crystal Oscillator).
84	PWR	GND

## NOTES

All Inputs and Outputs are TTL / +5V CMOS compatible.

Key To Above Table

N/C = No Connection

O/P = Output

I/P = Input

### **\*\*IMPORTANT\*\***

1. Do not connect N/C (No Connection) pins to any signal, ground or power – Leave them floating.
2. Although some power (PWR) pins are connected internally, it is important to individually connect all power pins to earth or power.
3. Ensure correct decoupling on all power pins. Recommended decoupling is an 0.1 uF capacitor and 6.8uF capacitor per +5V power pins. Failure to decouple properly will lead to random behaviour of the device (miscounting etc).

## Appendix 1

Pin out of device when fitted to a 84W PLCC socket (Plated through hole type).

